REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	9/23/99	FINAL 01 JUN 97 - 31 MAY 99

4. TITLE AND SUBTITLE

DYNAMIC THRESHOLD-VOLTAGE MOSFET

5. FUNDING NUMBERS

FDN00014-97-1-0699

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10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

a. DISTRIBUTION / AVAILABILITY STATEMENT

APPROVED FOR PUBLIC RELEASE

12. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

A Dynamic Threshold MOS (DTMOS) transistor has the unique ability to operate at 0.5V with high speed and current wile delivering a low off-state leakage. This project investigated the possibility of using DTMOS at Vdd>0.5V to achieve higher circuit performance.

14. SUBJECT TERMS

Low-power, CMOS

15. NUMBER OF PAGES

2

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
unclassified	unclassified	unclassified	UL

DYNAMIC THRESHOLD-VOLTAGE MOSFET

Professor Chenming Hu

1. OVERVIEW

In October 1994, we proposed the novel DTMOS technology that has a performance at 0.5V far exceeding what has been considered possible.

Reducing the power supply voltage is a very effective way of reducing the power consumption of IC's. The 1997 National Technology Roadmap for Semiconductors projected that the power supply voltage will scale with the channel length in direct proportion. Today's 0.25μm CMOS technology is powered by 2.5V power supplies. 1 volt power supply is projected for the 0.1μm technology. It is not clear whether CMOS technology can be scaled below 0.05μm and 0.5V because of a fundamental conflict between speed performance and power dissipation.

We proposed a revolutionary device innovation to satisfy both the high-speed and low-leakage requirements. We proposed to make V_T a function of the gate voltage, V_g. Specifically, V_T shall be low (0.1V) when the transistor is on $V_g = 0.5V$) so that circuit speed will be excellent; V_T will be high (0.4V) when the transistor is low ($V_g = 0V$) so that leakage current will be low too. This dynamic V_T is achieved by simply shorting the gate to the body. Implementation in SOI is straightforward because the body is otherwise electrically isolated; only a contact layout change is required to turn a conventional MOSFET into a DTMOS of either n or P channel type. SOI has the added benefit of being low in capacitance, which is good for low power operation, and being potentially superior to bulk technology in density (good for power too) and even manufacturability in the long run. DTMOS, however, can also be implemented in bulk using a triple well technology.

In this AASERT project, DTMOS was investigated for use with $V_{dd} > 0.5V$. To prevent the body-source to draw forward bias current, special circuit schemes need to be used.

2. BRIEF SUMMARY OF MAJOR CONTRACT ACCOMPLISHMENTS

It was demonstrated through circuit simulation that DTMOS is particularly attractive for low-voltage pass-gate logic circuits. Several circuits schemes were found to allow DTMOS operation at $V_{dd} > 0.5V$.

3. TECHNOLOGY TRANSFERRED

- DTMOS technology was transferred to IBM and AMD.
- DTMOS technology has been used at NTT, Toshiba and Sharp for 0.5V circuit design.